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whereby the gate of the first transistor and the gate of the third transistor are coupled together.

14. The pixel as recited in Claim 13, wherein said gate of said **[first transistor is at a first voltage and said first electrode of said first transistor is at a second voltage, said second electrode of said first transistor being connected to said photosensitive element, said gate of said]** second transistor is **[being]** connected to said third transistor.

a1

15. The pixel as recited in Claim 14, wherein **[said gate of said first transistor is at said first voltage and wherein]** one of said electrodes of said third transistor is connected to said gate of said second transistor and the other of said electrodes is connected to said first connection.

Please add the following new claim:

a2

16. The pixel as recited in Claim 13, whereby the gate of the first transistor and the gate of the third transistor are coupled to a DC voltage.

REMARKS

Please reconsider the application in view of the amendments and remarks, the Examiner rejected Claims 13-15 under 35 U.S.C. § 102(b). None of the cited references, Ricquier et al., Aw et al. or Buhler et al. disclose, teach, or suggest that the gate of the third transistor (49) is connected to the gate of the first transistor (47). At least this characteristic is novel over all three references.

In Ricquier et al the gate of the first transistor (M1) is connected to a positive supply (VDD), and the gate of the third transistor (M2) is coupled to the connection between the first transistor (M1) and the photodiode. In Aw et al., the gate of the first transistor (M4) is connected to a signal Reset, and the gate of the third transistor (M3) is connected to a signal shutter. Both signals are different. In Aw et al. the pixel array is held in a reset state until the shutter control goes high. In Buhler et al., a diode reset signal ϕ_{DR} is applied to the gate of the first transistor (M1), while a transfer gate voltage signal V_{T1} is applied to the gate of the third transistor (M2). Accordingly, none of the cited documents discloses, teaches, or suggest applying the same voltage level to the gates of both the first and the third transistor.

Support for the characteristic of coupling the gates of the first and the third transistor together can be found in Fig. 4, and in the description, at P.7:27-P.8:2.

In view of the foregoing amendments and remarks, the claims are believed to be in condition for allowance and such allowance is earnestly requested. If any issues remain to be resolved, the Examiner is invited to contact the undersigned in order to promptly resolve any such issues.

Respectfully submitted,

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